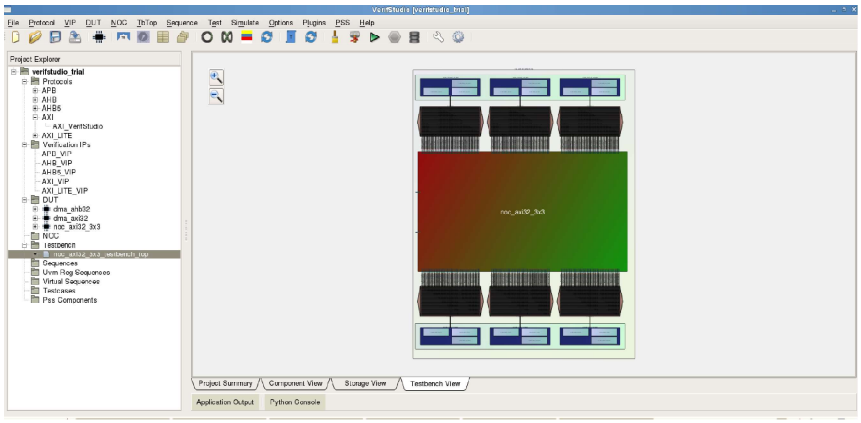
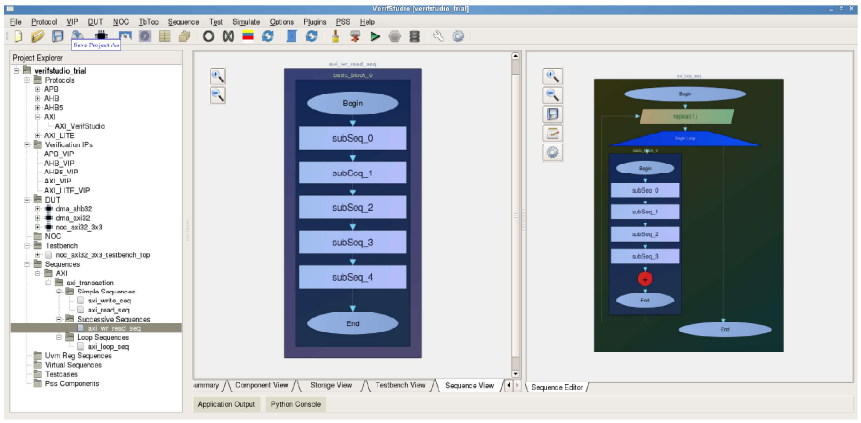
VerifStudio

Save time and effort on your UVM based block level verification

- ✓ Automatic creation of complex UVM testbench environments for
  - ❍ Block level verification
  - ❍ Bus Integration verification
- ✓ Creation of hierarchical sequences and tests using
  - ❍ A powerful Python API
  - ❍ Graphical sequence-editor
- ✓ Well-commented easy-to-read UVM code
  - ❍ Widely accepted coding practices
- ✓ Works with any VIP of your choice
- ✓ Easily integrates UVM Reg model
- ✓ Creates functional coverage models



UVM Testbench Builder



UVM Hierarchical Sequence Editor

VERIFICATION · PRODUCTIVITY · IMPROVEMENT

INTERESTED IN A TEST-DRIVE?
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Verification Productivity Solutions

VERIFICATION PRODUCTIVITY IMPROVEMENT

VerifStudio

An innovative approach to UVM based block level verification

BENEFITS

- ✓ Automates the creation of UVM Testbenches
- ✓ Block based architectures using VIPs
- ✓ NOC based architectures
- ✓ Works with 3rd party VIPs
- ✓ Generates templates and connectivity of Scoreboards
- ✓ Highly interactive graphical interface for Sequence and Test-case creation
- ✓ Enables setting of UVM Config Db parameters for each VIP Agent
- ✓ Easy integration and configuration of Clock/Reset drivers
- ✓ Integration of UVM REG model into the UVM environment
- ✓ Generates well-documented easy-to-read System Verilog Code
- ✓ Widely accepted coding practices
- ✓ Allows compilation and simulation of testcases from tool interface
- ✓ Automatically refactors generated code when parameters change
- ✓ A powerful python based API supports all UVM creation operations
- ✓ Enables easy creation of functional coverage models
- ✓ Supports automatic generation of project documentation

Just focus on scenarios...
Leave the UVM to us!

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